

Appl. No. 09/452,691  
Reply to Office action of 01/12/2004

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claim 1 (previously amended): An integrated circuit comprising:

- a lower metal interconnect layer located over a semiconductor body;
- a multi-level dielectric layer located over said lower interconnect layer;
- an upper metal interconnect layer located over said multi-level dielectric layer;

and

- a thin film resistor embedded within said multi-level dielectric layer between said lower metal interconnect layer and said upper metal interconnect layer, wherein said thin film resistor comprises a resistor layer that is physically separated, in its entirety, in a vertical direction from any metal interconnect layer.

Claim 2 (previously presented): The integrated circuit of claim 1, further comprising:

- a first via extending from said upper metal interconnect layer to said lower interconnect layer; and
- a second via extending from said upper metal layer to said thin film resistor.

Claim 3 (original): The integrated circuit of claim 1, wherein said thin film resistor comprises a hard mask located over an end of the thin film resistor.

Claim 4 (cancelled).

Claim 5 (cancelled).

Claim 6 (original): The integrated circuit of claim 1, wherein said thin film resistor comprises TaN.

Appl. No. 09/452,691  
Reply to Office action of 01/12/2004

Claim 7 (original): The integrated circuit of claim 1, wherein said thin film resistor comprises SiCr.

Claim 8 (original): The integrated circuit of claim 1, wherein said thin film resistor comprises NiCr.

Claims 9-18 (cancelled)

Claim 19 (previously presented): An integrated circuit comprising:

- a first metal interconnect layer;
- a second metal interconnect layer located over said first metal interconnect layer, there being no additional metal interconnect layers between said first and second metal interconnect layers;
- a multi-level dielectric layer located between said first metal interconnect layer and said second metal interconnect layer; and
- a thin film resistor embedded within said multi-level dielectric layer between said first metal interconnect layer and said second metal interconnect layer such that said multi-level dielectric layer separates said thin film resistor from both said first metal interconnect layer and said second metal interconnect layer.

Claim 20 (previously presented): The integrated circuit of claim 19, wherein the integrated circuit further comprises:

- a first plurality of conductively filled vias extending from said second metal interconnect layer to said first interconnect layer; and
- a second plurality of conductively filled vias extending from said second metal layer to said thin film resistor.

Appl. No. 09/452,691  
Reply to Office action of 01/12/2004

**Claim 21 (new): An integrated circuit comprising:**

- a lower metal interconnect layer located over a semiconductor body;
- a multi-level dielectric layer located over said lower interconnect layer;
- an upper metal interconnect layer located over said multi-level dielectric layer;

**and**

a thin film resistor embedded within said multi-level dielectric layer between said lower metal interconnect layer and said upper metal interconnect layer, wherein said thin film resistor comprises a resistor layer that is physically separated, in its entirety, in a vertical direction from any metal interconnect layer, wherein said thin film resistor comprises a hard mask located over an end of the thin film resistor, and wherein said hard mask comprises TiW.

**Claim 22 (new): An integrated circuit comprising:**

- a lower metal interconnect layer located over a semiconductor body;
- a multi-level dielectric layer located over said lower interconnect layer;
- an upper metal interconnect layer located over said multi-level dielectric layer;

**and**

a thin film resistor embedded within said multi-level dielectric layer between said lower metal interconnect layer and said upper metal interconnect layer, wherein said thin film resistor comprises a resistor layer that is physically separated, in its entirety, in a vertical direction from any metal interconnect layer, wherein said thin film resistor comprises a hard mask located over an end of the thin film resistor, and wherein said hard mask comprises TiN.